* Motorola 68000 (m68k) Architecture
	+ Intro and History:
		- First introduced in 1979 in HMOS technology. Desktop processors competing with Intel x86 (8086, 8088, 80286).
		- Found in early Atari, Amiga, and Macintosh computers through the 1980's and 90's
		- Still found in embedded systems
		- 32 bit CISC architecture
		- Also was used in first post-script printers created by Adobe
		- Some consider it to be a successor to the PDP-11 or VAX, and is in many ways a 32 bit version of the PDP-11
		- Great at running C code and was big in the UNIX market, including SUN and SGI IRIS workstations
		- Motorola stopped development of 68k architecture in 1994, replacing it with the PowerPC architecture.
	+ Instruction Set Design
		- On the original 68000 there are 56 instructions at a minimum size of 16 bits
		- 16/32 bit CISC instruction set
			* 32 bit instruction set, registers, and internal data bus
			* 16 bit ALU and external data bus on the original, 32 bit on later CPU's
		- Does not have an equivalent to CPUID on x86
		- Nearly Orthogonal Instruction set design
			* don't have different instructions for accessing from memory or registers, many instructions can access either or with addressing mode specifiers.
			* Almost all address modes are available for almost all instructions
			* More common in CISC instruction sets, and makes it easier to program in assembly because you just need to know a few instructions and a few addressing modes instead of many different instructions that all functionally do the same things.
			* From an assembly level it looks orthogonal, but from a bit level, and from the view of the CPU designers it is not
				+ this gives a good compromise, easy for programmers, and cpu designers can make it more efficient.
		- many believed the system had compact code for it's cost, and made design wins for the architecture.
			* Provided longevity, especially in embedded systems until ARM introduced compressed thumb op-codes
		- Most instructions are dyadic: have source and destination and result is placed in destination
		- Number of cycles for an instruction can depend on the source of the instructions data.
	+ Datapath Design
		- The first CPU in the series to feature a true cache was the 68020, with 256 bytes.
		- 68020 was also the first to have a proper three stage pipeline
		- Big Endian
		- 8 32 bit data registers, 7 32 bit address registers
		- Last address register also is the stack pointer 32 bit PC counter
		- Considered good amount of registers for the time
			* Meant could respond fast to interrupts, because at most it only had to store 15 registers
			* Could also do most calculations fast, because the calculations can be done within the CPU, don't need to go to main memory to get data
		- System also has a status register for bit flags such as zero, carry, overflow, extend, and negative.
		- Two Privilege Levels
			* CPU has two privilege levels, those are user and supervisor mode
			* User mode gives access to everything except interrupt level controls
			* Supervisor Bit stored in status register and is visible to even user programs
			* Supervisor has a separate stack pointer than user. permits a very small level of multitasking
	+ Memory Subsystem Design
		- Original 68000 had 24 bit external address bus, so could only address 16MB of memory
			* Internally, architecture has 32 bit memoery address bus
				+ design was to future proof the system and make software forward compatable
		- Later 68k CPU's had 32 bit external address bus so that system could address up to 2GB
	+ HPC
		- Starting with 68020, CPU could support multiple co-processors
		- Multiprocessing support implimented through TAS, CAS, and CAS2 on the 68020
		- Comparisons to IA